

REMARKS

This AMENDMENT UNDER 37 CFR 1.111 is filed in reply to the outstanding Office Action of March 14, 2003, and is believed to place this case in condition for allowance for the following reasons.

OK
Initially, substitute Figures 1A, 1B, 1C, 1D, 1E and 1F are attached hereto which add the legend PRIOR ART thereto, as proposed in the previous AMENDMENT.

Responsive to the objection in paragraph 1 of the Official Action, "body contact" has been changed to – body region – in claim 1, which is believed to obviate this objection.

Responsive to the objection in paragraph 2 of the Office Action, claim 2 has been cancelled.

Reconsideration is respectfully requested of the rejection of claims 1 and 3-5 under 35 U.S.C. 102(e) as being allegedly anticipated by Gruening et al (U.S. patent no. 6,437,381).

The last two subparagraphs of claim 1 specify (with reference numerals to the present invention added for easy reading on the drawings).

a trench top oxide (TTO) layer (28) formed on a horizontal surface of the DRAM cell array for isolating the deep trench conductor (22) forming an electrode of said underlying capacitor and said buried-strap outdiffusion region (24 near 26) from a gate conductor region (32);

an underlying nitride layer (50) formed between a top of said deep trench conductor (22) and said buried-strap outdiffusion region (24 near 26) and underlying said TTO layer (28) to eliminate a possibility of TTO layer dielectric breakdown between said gate conductor region (32) and said electrode of said underlying capacitor.

The Examiner has attempted to read these limitations on Gruening et al as follows, with reference numerals of Gruening et al added thereto.

a trench top oxide (TTO) layer (160) formed on a horizontal surface of the DRAM cell array for isolating the deep trench conductor (36) forming an electrode of said underlying capacitor and said buried-strap outdiffusion region (62) from a gate conductor region (gate electrode on top of gate oxide 160);

an underlying nitride layer (1250) formed between a top of said deep trench conductor (36) and said buried-strap outdiffusion region (62) and underlying said TTO layer (160) to eliminate a possibility of TTO layer dielectric breakdown between said gate conductor region and said electrode (36) of said underlying capacitor.

In the above reading and analysis, the Examiner has read the TTO layer of the claim as layer 160 of Gruening even though Gruening et al refers to the TTO layer as layer 14, and one skilled in the art would consider the TTO layer as layer 14.

However, to avoid any question that claim 1 reads on Gruening et al, claim 1 has been amended to specify that the underlying nitride layer (50) is formed immediately adjacent to and contacting a top of said deep trench conductor, which avoids reading on Gruening et al since in Gruening et al the TTO layer 14 is formed immediately adjacent to and

contacts the top of the deep trench conductor, and the nitride layer is formed on top of the TTO layer 14.

New claim 16 has been added to further distinguish the present invention from the prior art, wherein Gruening et al discloses a nitride layer 1250 which is formed over the entire structure as shown in Figure 15.

This application is now believed to be in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,

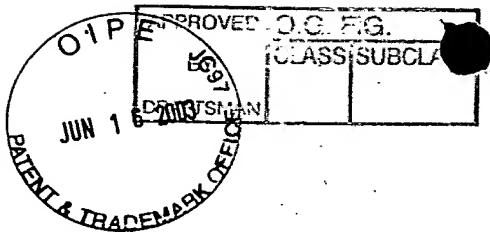


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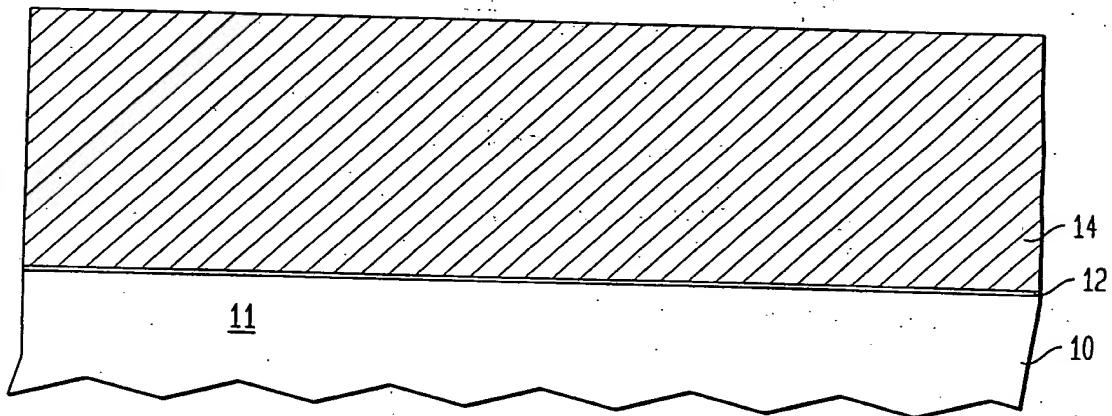
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Enclosures



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THOMAS W. DYER, et al.
F1S920000337US1 (TMCL)

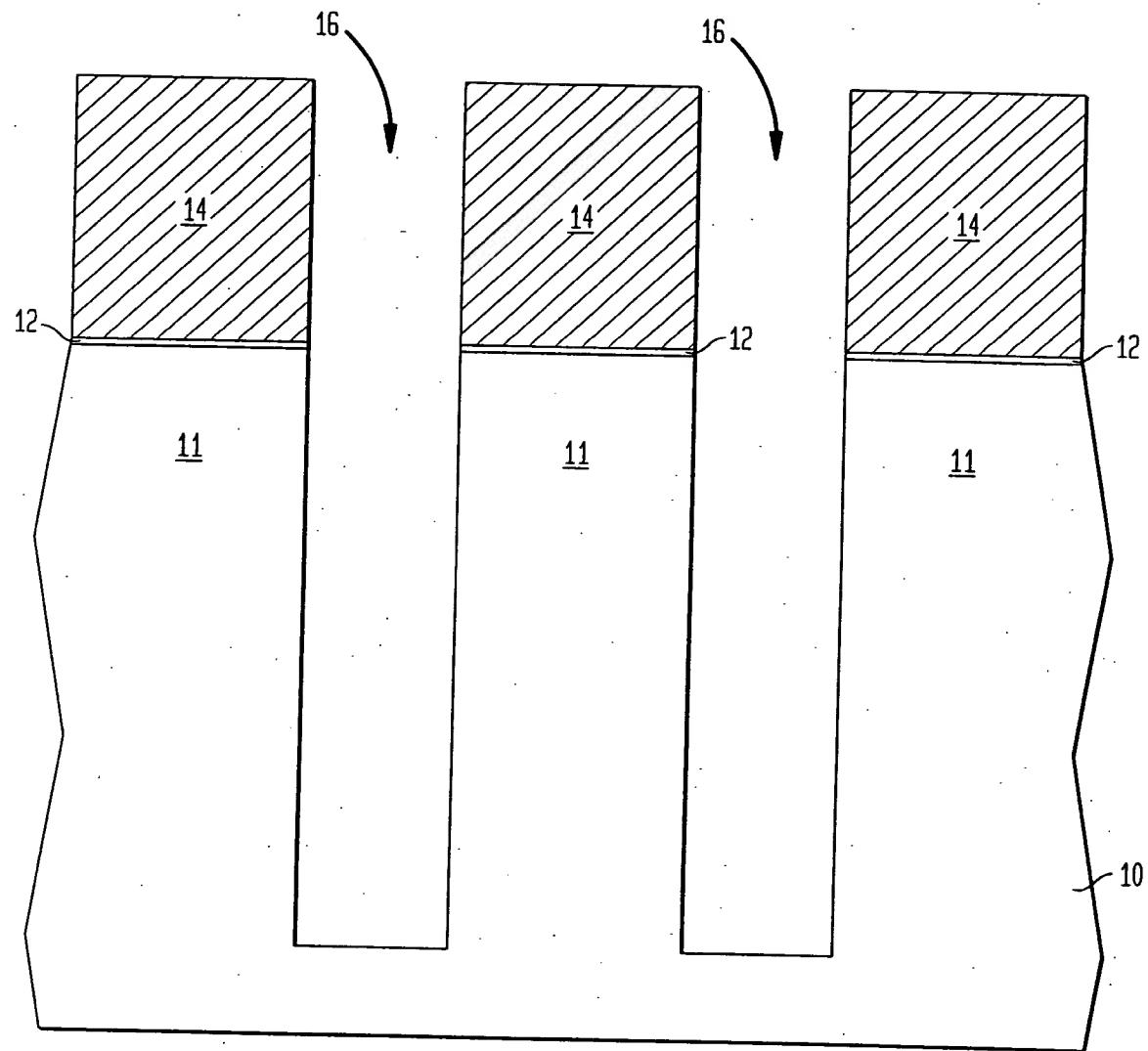
FIG. 1A PRIOR ART

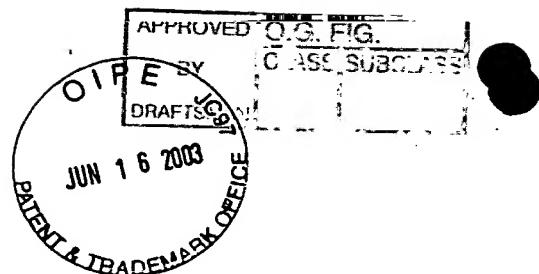




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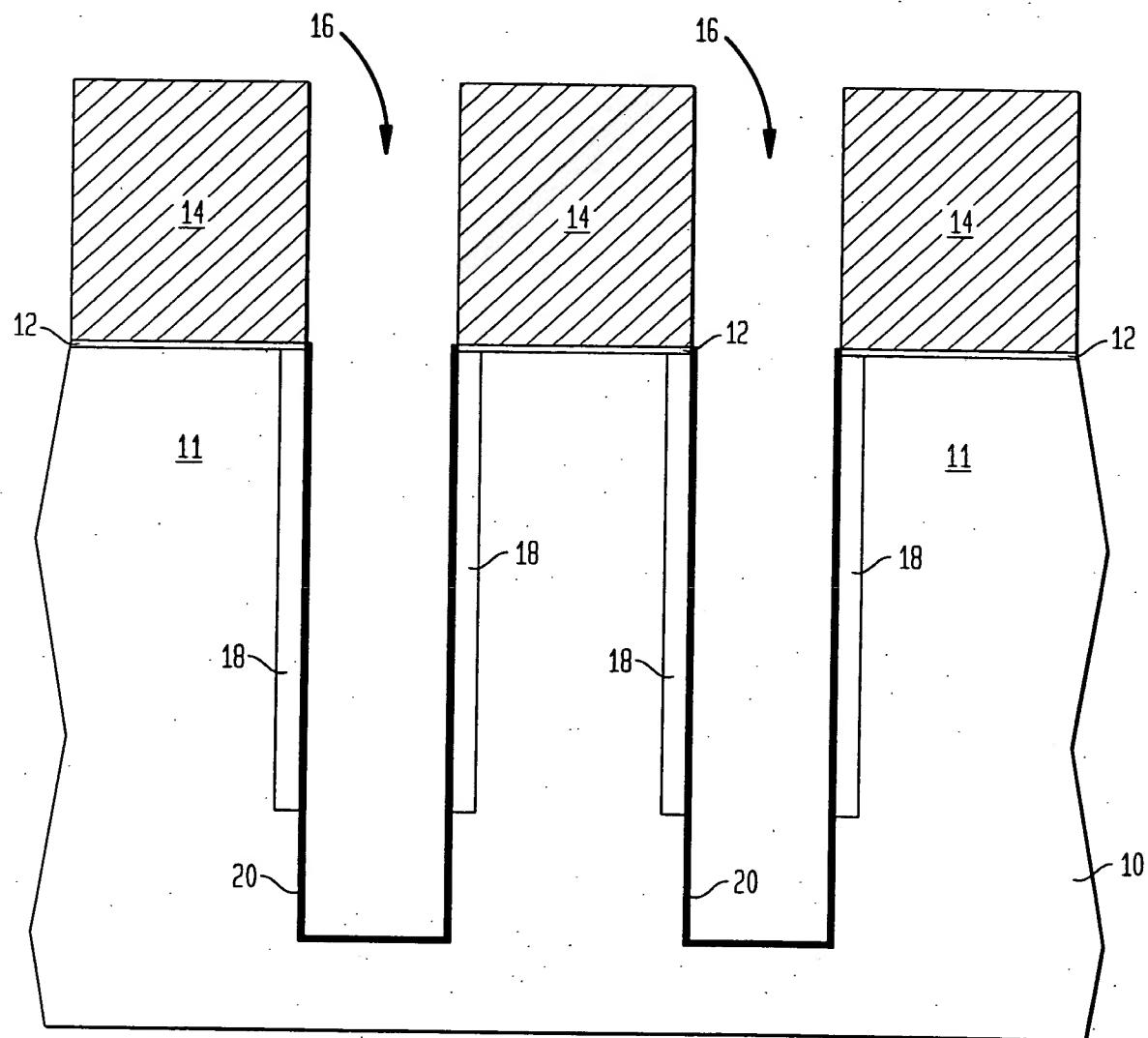
FIG. 1B PRIOR ART

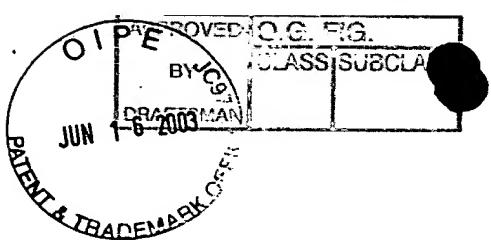




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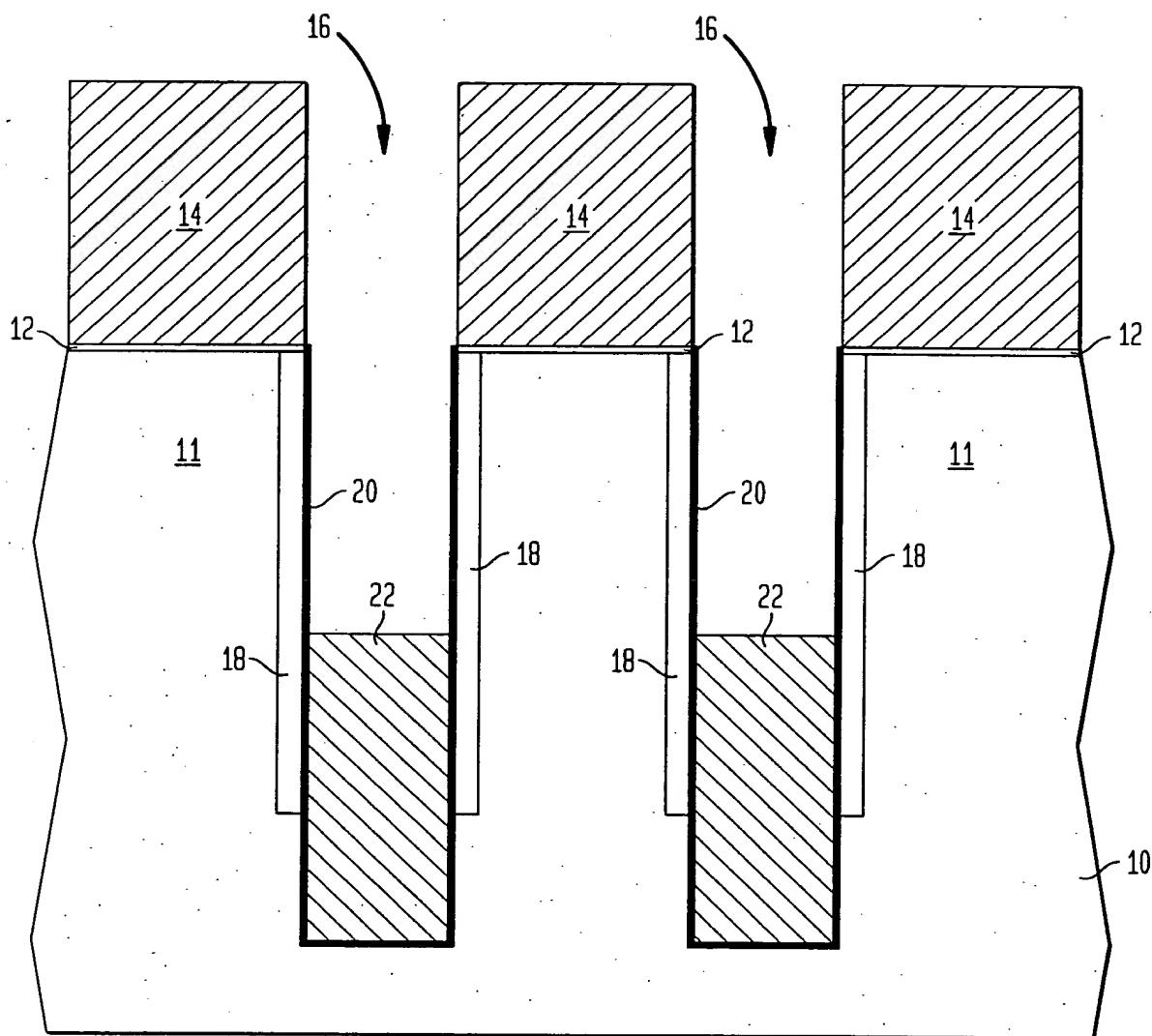
FIG. 1C PRIOR ART





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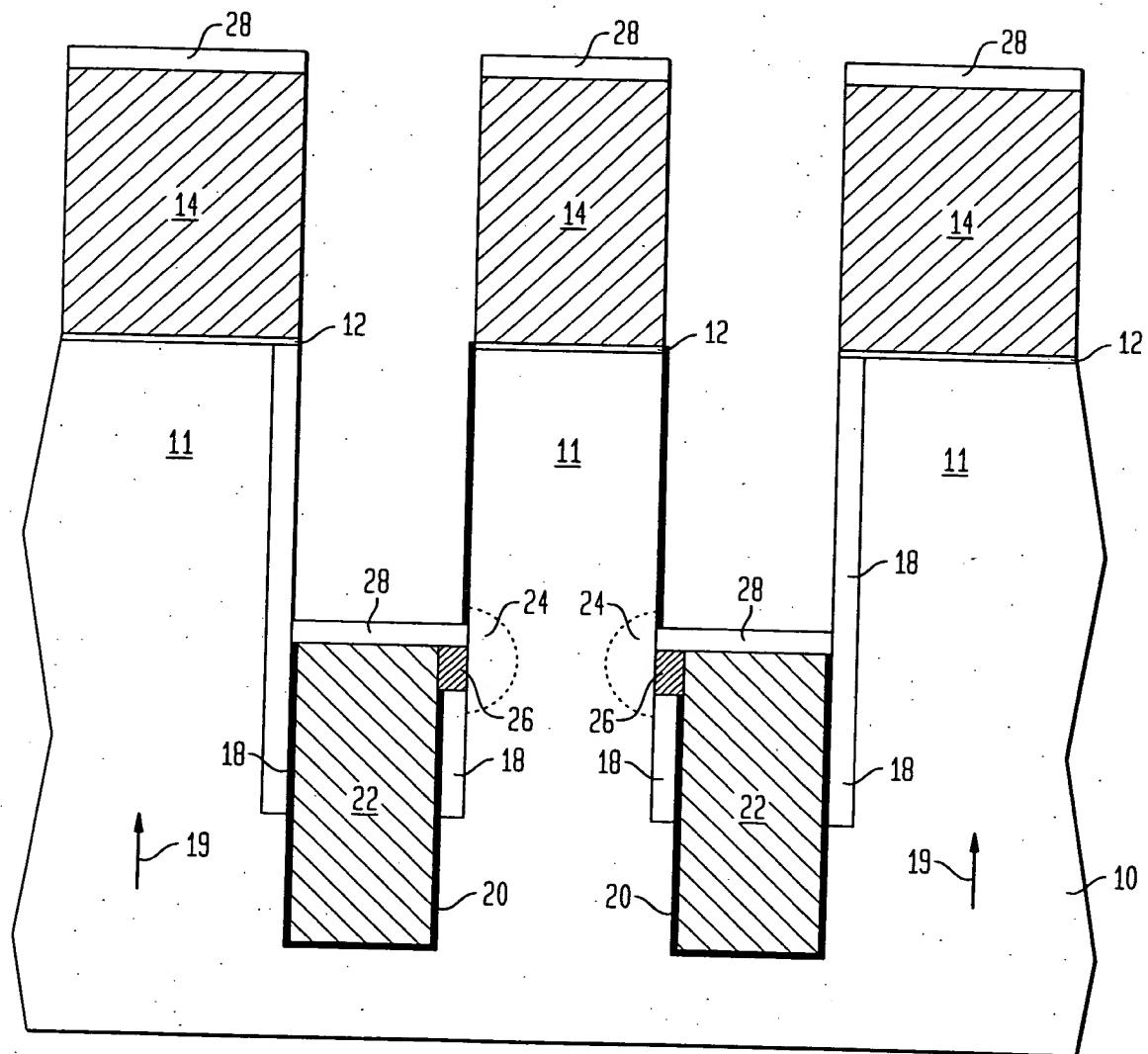
FIG. 1D PRIOR ART





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FIG. 1E PRIOR ART





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FIG. 1F PRIOR ART

